I CLAIM

1. A data processing apparatus, comprising:

a first bus for coupling a first master logic unit with a plurality of slave logic units to enable the first master logic unit to issue a first transfer request to any of said slave logic units;

a second bus for coupling a second master logic unit with a subset of said plurality of slave logic units to enable the second master logic unit to issue a second transfer request to any of the slave logic units in said subset; and

a slave interface mechanism associated with each slave logic unit in said subset and comprising switching logic arranged to connect either the first bus or the second bus to the corresponding slave logic unit to enable either the first transfer request or the second transfer request to be routed to that slave logic unit.

2. A data processing apparatus as claimed in Claim 1, wherein the slave interface mechanism comprises an arbitration control unit for applying predetermined criteria to control the routing of the first and second transfer requests to the corresponding slave logic unit in the event that the slave logic unit is already processing one of the transfer requests when the other transfer request is issued to the slave logic unit.

3. A data processing apparatus as claimed in Claim 2, wherein the first and second transfer requests are burst transfer requests, each burst transfer request comprising a non-sequential transfer request followed by a number of sequential transfer requests, and the predetermined criteria applied by the arbitration control unit is such that upon issuance of a non-sequential transfer request from one of said master logic units, the slave interface mechanism will defer routing that non-sequential transfer request to the slave logic unit until any burst transfer request already being handled by that slave logic unit has been completed.

4. A data processing apparatus as claimed in Claim 3, wherein the slave logic unit is arranged to issue an acknowledge signal to confirm that a current transfer request has been performed, each master logic unit being arranged to await receipt of the

acknowledge signal before issuing a subsequent transfer request, and the arbitration control unit being arranged to withhold the acknowledge signal output to the master logic unit issuing the deferred non-sequential transfer request to ensure that the master logic unit keeps asserting that non-sequential transfer request until the slave logic unit is available to receive it.

5. A data processing apparatus as claimed in Claim 2, wherein the first and second transfer requests are burst transfer requests, each burst transfer request comprising a non-sequential transfer request followed by a number of sequential transfer requests, and the predetermined criteria applied by the arbitration control unit is such that upon issuance of a non-sequential transfer request from one of said master logic units, the slave interface mechanism may route that non-sequential transfer request to the slave logic unit without waiting until any burst transfer request already being handled by that slave logic has been completed.

6. A data processing apparatus as claimed in Claim 5, wherein each master logic unit is arranged to issue as part of each transfer request a control signal indicating the type of transfer request, and the arbitration control unit is arranged to manipulate that control signal prior to it being output to the corresponding slave logic unit to enable a burst transfer request to be split into a number of shorter length burst transfer requests.

7. A data processing apparatus as claimed in Claim 5, wherein the predetermined criteria specify relative priorities for each master logic unit, and this priority information is used by the arbitration unit to determine upon issuance of a non-sequential transfer request from one of said master logic units whether to interrupt a burst transfer request already being handled by that slave logic unit.

8. A data processing apparatus as claimed in Claim 5, wherein the predetermined criteria specify a maximum length of a burst transfer request, such that if, upon issuance of a non-sequential transfer request from one of said master logic units, a burst transfer request already being handled by that slave logic unit has reached said maximum length, the slave interface mechanism is arranged to route that non-sequential transfer request to

the slave logic unit without waiting for the burst transfer request already being handled by that slave logic to complete.

9. A data processing apparatus as claimed in Claim 1, wherein the slave interface mechanism comprises a buffer for temporarily storing a transfer request issued to the corresponding slave logic unit from one of said master logic units if another transfer request is already being handled by that slave logic unit.

10. A data processing apparatus as claimed in Claim 4, wherein the slave interface mechanism comprises a buffer for temporarily storing a transfer request issued to the corresponding slave logic unit from one of said master logic units if another transfer request is already being handled by that slave logic unit, and wherein the non-sequential transfer request comprises a first part issued in a first clock cycle and a second part issued in a second clock cycle, the buffer being arranged to store the first part of the non-sequential transfer request, and the arbitration control unit being arranged to withhold in the second clock cycle the acknowledge signal output to the master logic unit issuing the deferred non-sequential transfer request to ensure that the master logic unit keeps asserting the second part of the non-sequential transfer request until the slave logic unit is available to receive it.

11. A slave interface mechanism for a data processing apparatus as claimed in Claim 1, the slave interface mechanism including a first connection for connecting to the first bus, a second connection for connecting to the second bus and a third connection for enabling the corresponding slave logic unit to be coupled to the slave interface mechanism, the slave interface mechanism comprising switching logic arranged to connect either the first bus or the second bus to the corresponding slave logic unit to enable either the first transfer request or the second transfer request to be routed to that slave logic unit.